

FREQUENCY RESPONSE OF TWO STAGE CASCADED EMITTER COUPLED AMPLIFIER

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ABSTRACT

The Common Emitter Amplifier is one of the three basic transistor amplifier configurations. In this work, a basic NPN common emitter transistor amplifier is built and investigated. It is then coupled with similar Common Emitter transistor amplifier in an emitter coupled format. Then, the first stage emitter couple is cascaded with a second one. Frequency responses for the two circuits are also determined. The results show that cascading shrunk the bandwidth but enhance the overall gain.

KEYWORDS: Common emitter, Emitter Coupled amplifier, Common mode rejection rati

INTRODUCTION

The transistor is a solid state device, whose operation depends upon the flow of electric charge carriers within the solid. Transistor is capable of amplification and in most respect it is analogous to a vacuum triode. The main difference between the two is that the transistor is a current controlled device whereas vacuum triode is a voltage controlled device. The transistor is only about 5 decade old, yet it is replacing vacuum tubes in almost all applications. The reasons are obviously its advantages over vacuum tubes such as compact size, light weight, rugged construction, more resistive to shocks and vibrations, instantaneous operation (on heating required), low operating voltage high operating efficiency (no heat loss) and long life with essentially no ageing effect if operated within permissible limits of temperature and frequency. However, transistors, in comparison to vacuum triodes, have some drawbacks also such as loud hum noise,

restricted operating temperature (upto 75°C) and operating frequency (upto a few MHz only).

It consists of a silicon or germanium (preferably silicon because of its smaller cut-off current ICBO, smaller variations in ICBO due to variations in temperature and higher operating temperature) Cristal in which a layer of N-type material is sandwiched between two layers of P-type material. [1] NPN is one of the two types of bipolar transistors, consisting of a layer of P-doped semiconductor (the "base") between two N-doped layers. A small current entering the base is amplified in the collector output. That is, an NPN transistor is "on" when its base is pulled high relative to the emitter.

METHODOLOGY

Design and Simulation

In this section the designed procedure of an amplifier and the design equation used in this research work was presented. The procedure, in which the design circuit was tested, was simulating method.

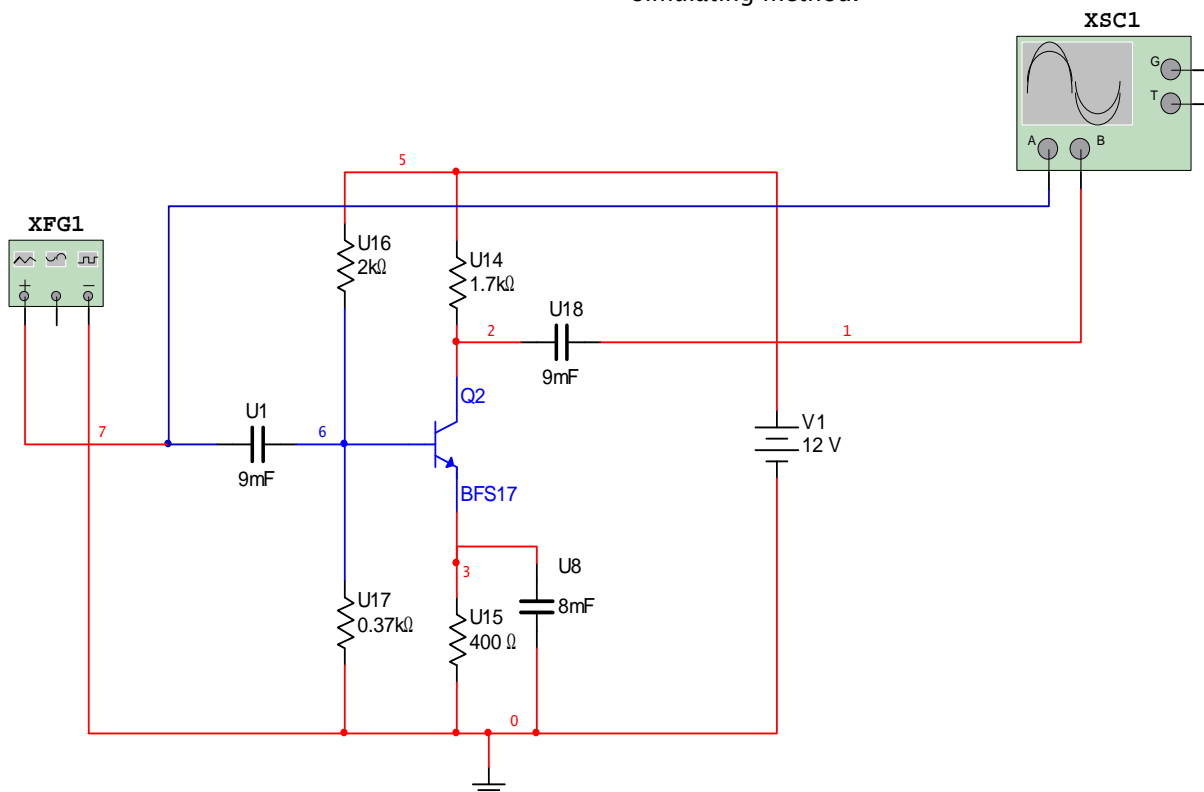


FIGURE 2.1 Amplification of Common Emitter transistor amplifiers.

Design procedure

The amplifier circuit used in this research work was designed from BFS17 transistor which was selected from the transistor family. The choice of the transistor was due to the fact that, it was an NPN transistor with high forward current gain, small saturation current and as well it availability.

By selecting the transistor, the output characteristics of the transistor was determined by computer simulation using multism 8 software. Using the data, the output characteristics curves were drawn.

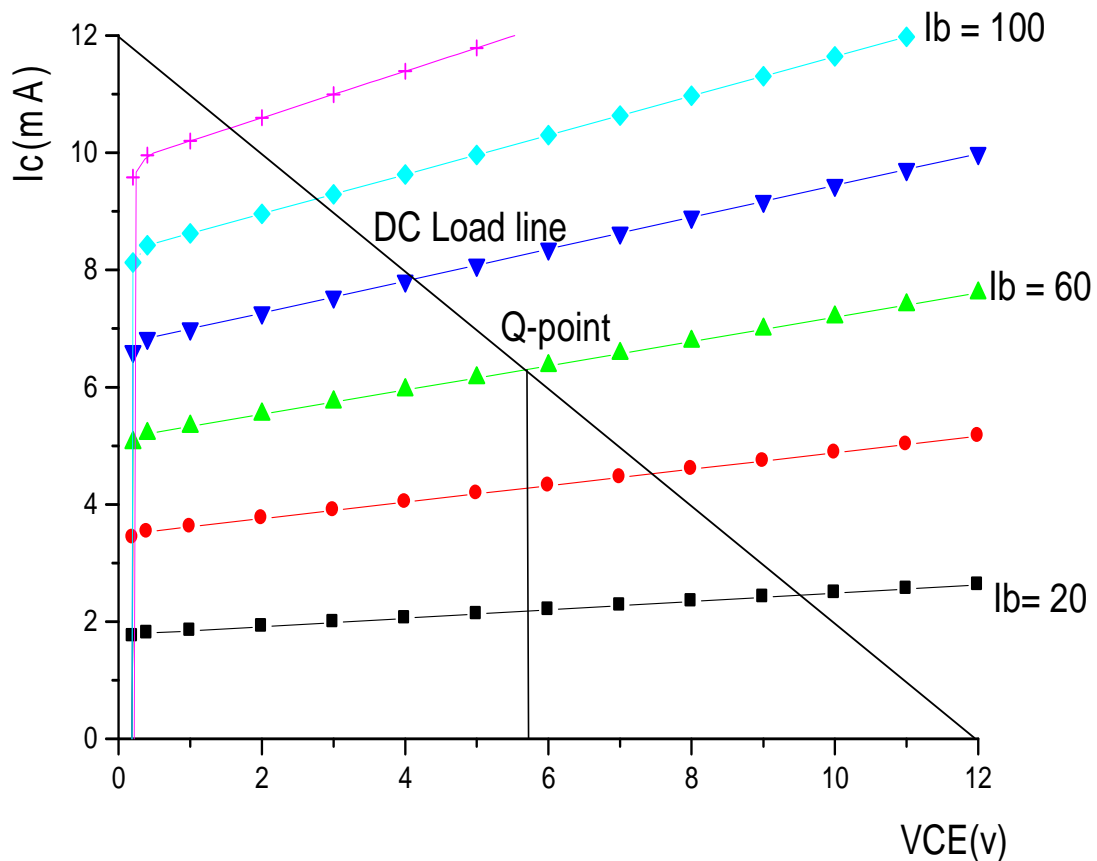


FIGURE 2.2 A GRAPH OF I_c (mA) OF AGAINST V_{CE} (V)

From the output characteristics curves, the bias voltage V_c the biasing resistors and capacitors were determined. The V_{cc} (dc supply) battery was chosen along the V_c axis. The bias voltage V_{ce} was approximated to be $\frac{1}{2} V_{cc}$. By selecting a particular value of I_b , the operating point called Q-point was located as the intersection of the selected values. The value of I_c at the Q-point was directly obtained from the curve. Knowing the values of I_c , V_{cc} , V_{ce} , and I_b , the biasing resistors were determined. V_e was approximately $\frac{1}{10} V_{cc}$ and using ohm's law

$$R_e = \frac{V_e}{I_e} \tag{3.1}$$

With $I_e = I_c$ and from the output loop

$$R_c = \frac{V_{cc} - V_{ce} - V_e}{I_c} \tag{3.2}$$

The C-E current amplification factor,

$$\beta = \frac{I_C}{I_B} \quad (3.3)$$

The base biasing voltage $V_{BB} = V_E + V_{BE}$ (3.4), ($V_{BE} = 0.7$ for silicon)

$$R_{B2} = \frac{1}{10} \beta R_E \quad (3.5)$$

Where $R_{E} = V_{CC} / 10 I_{C_{from}}$ potential divider [2]

From potential divider

$$R_{B1} = \frac{(R_{B2} \times V_{CC} - R_{B2} \times V_{BB})}{V_{BB}} \quad (3.6)$$

The coupling capacitor C_{in} and the emitter bypass capacitor C_E were obtained from [3]

$$C_{in} = \frac{1}{2 \pi f R_{B2}} \quad (3.7)$$

And

$$C_E = \frac{1}{2 \pi f R_E} \quad (3.8)$$

Many electronic devices use differential amplifiers internally. The output of an ideal differential amplifier is given by:

$$V_{out} = A_d (V_{in}^+ - V_{in}^-) \quad (3.8a)$$

Where V_{in}^+ and V_{in}^- are the input voltages and A_d is the differential gain. In practice, however, the gain is not quite equal for the two inputs. This means, for instance, that if V_{in}^+ and V_{in}^- are equal; the output will not be zero, as it would be in the ideal case.

$$V_{out} = A_c \left(\frac{V_{in}^+ + V_{in}^-}{2} \right) \quad (3.8b)$$

A_c is called the common-mode gain of the amplifier.

Differential amplifiers are often used when it is desired to null out noise or bias-voltages that appear at both inputs, a low common-mode gain is usually considered good.

Hence, for the practical differential amplifier, the output of differential amplifier is given by:

$$V_{out} = A_d (V_{in}^+ - V_{in}^-)$$

The common-mode rejection ratio, usually defined as the ratio between differential-mode gain and common-mode gain, indicates the ability of the amplifier to accurately cancel voltages that are common to both inputs. Common-mode rejection ratio (CMRR):

$$CMRR \triangleq \frac{A_d}{A_c} \quad (3.8c)$$

In a perfectly symmetrical differential amplifier, A_c is zero and the CMRR is infinite. Note that a differential amplifier is a more general form of amplifier than one with a single input; by grounding one input of a differential amplifier, a single-ended amplifier results. One of the more common features of a differential amplifier is its ability to cancel out or reject certain types of undesired voltage signals. Such undesired signals are referred to as "noise" and may occur owing to voltages induced by stray magnetic fields in the ground or signal wires, as voltage variations in $\Delta V = V_o / V_{in}$

Also, $AV = gmRc$

the voltage supply. Here the important point is that these noise signals are not the signals that are desired to be amplified in the differential amplifier. Their distinguishing feature is that the noise signal appears equally at both inputs of the circuit. It means that any undesired (or noise) signals that appear in polarity or common to both inputs terminals, will be largely rejected, or cancelled out at the differential amplifier output. The signal that is to be amplified appears at only one input or opposite in polarity at both inputs. Now what is important to be considered is that, if undesirable noise does not occur, up to what extent it is rejected out by the differential amplifier? A measure of this rejection of signals common to both inputs is referred to as the common-mode rejection of the amplifier and a numerical value is assigned, what is called the common-mode rejection ratio (CMRR) [4].

Simulation

Using the design equation (3.1) to (3.8) above the amplifier circuit was designed. The frequency responses of the circuits were obtained by measuring the output wave form displaced in an oscilloscope by simulation. The input signal was applied across the base and output was taken across the collector for given ranges of frequencies. The response of the amplifier was determined by evaluating the voltage gain as:

$$(3.9)$$

$$(3.10)$$

$$g_m = I_{CQ}/V_T \quad (3.11)$$

$$I_{CQ} = V_{CC}/2R_C \quad (3.12)$$

$$R_C = V_{CC}/2I_{CQ} \quad (3.13)$$

$$\text{Since, } A_V = -I_{CQ}/V_T \cdot V_{CC}/2I_C \quad (3.14)$$

$$A_V = -V_{CC}/2V_T \quad (3.15)$$

I_{CQ} = quiescent collector current.

V_T = voltage in B-E circuit (Transistor Voltage)

I_{CQ}/V_T = Conductance

But, conductance relates a current in collector to a voltage in the B-E circuit, the parameter is called TRANSCONDUCTANCE and is written as $g_m = I_{CQ}/V_T$ [5]

The vector sum of $V_{Resistance}$ and $V_{Capacitor}$. $V = I\sqrt{R^2 + X^2}$

$$V_{out} = I_C \sqrt{R^2 + X^2}$$

$$V_{out} = 3 \times 10^{-3} A \sqrt{(1.7K\Omega)^2 + ([0.37K\Omega]I)^2} = 137V$$

$$V_{in} = I_B \sqrt{R_{B2}^2 + X_B^2}$$

$$V_{in} = 60\mu A \sqrt{(2K\Omega)^2 + ([0.37K\Omega]I)^2} = 3V$$

But, voltage gain by calculation from the circuit above was found to be

$$A_V = \frac{V_{out}}{V_{in}} = \frac{137V}{3V} = 46$$

Hence, by comparison of the above calculated voltage gain value and the simulation voltage gain value

$$A_d = \frac{V_{out}}{V_{in} - V_o} = \frac{40}{1 - 0} = 40$$

Measurements

Table 3.1 A voltage amplification gain of different types of amplifier.

S/N	TYPE OF AMPLIFIER	V_{in}	V_{out}	$A_V = \frac{V_{out}}{V_{in}}$
1	Common Emitter transistor amplifier	1	40	4
2	Emitter Coupled amplifier before modification	1	55	55
3	Cascaded Emitter Coupled amplifier before modification	20	1.5	0.075
4	Emitter Coupled amplifier after modification	5	75	15
5	Cascaded Emitter Coupled amplifier after modification	10	40	4
6	Further modifications of cascaded Emitter Coupled amplifier	10	40	4

TABLE 3.2 The common-mode rejection ratio, CMRR of different types of amplifier.

S/N	TYPE OF AMPLIFIER	$A_c = \frac{2V_{out}}{V_{in} + V_o}$	$A_d = \frac{V_{out}}{V_{in} - V_o}$	CMRR = $\frac{A_d}{A_c}$
1	As one above	80	40	0.5
2	As two above	110	55	0.5
3	As three above	0.1	0.05	0.5
4	As four above	30	15	0.5
5	As five above	8	4	0.5
6	As six above	8	4	0.5

Table 3.3 SIMULATION MEASUREMENTS WITH BFS17 TRANSISTOR

S/N	Amplifier	Mid Gain/dB	$\frac{W_1}{Hz}$	$\frac{W_2}{Hz}$	Bandwidth/Hz	Gain Bandwidth product/Hz
1	As one above	30.05394	4500	24000	19500	586051.830
2	As two above	30.96909	7000	21200	14200	439761.078
3	As four above	31.79695	7400	22600	15200	483313.640
4	As five above	32.55272	7700	19700	12000	390632.640

RESULTS AND DISCUSSIONS

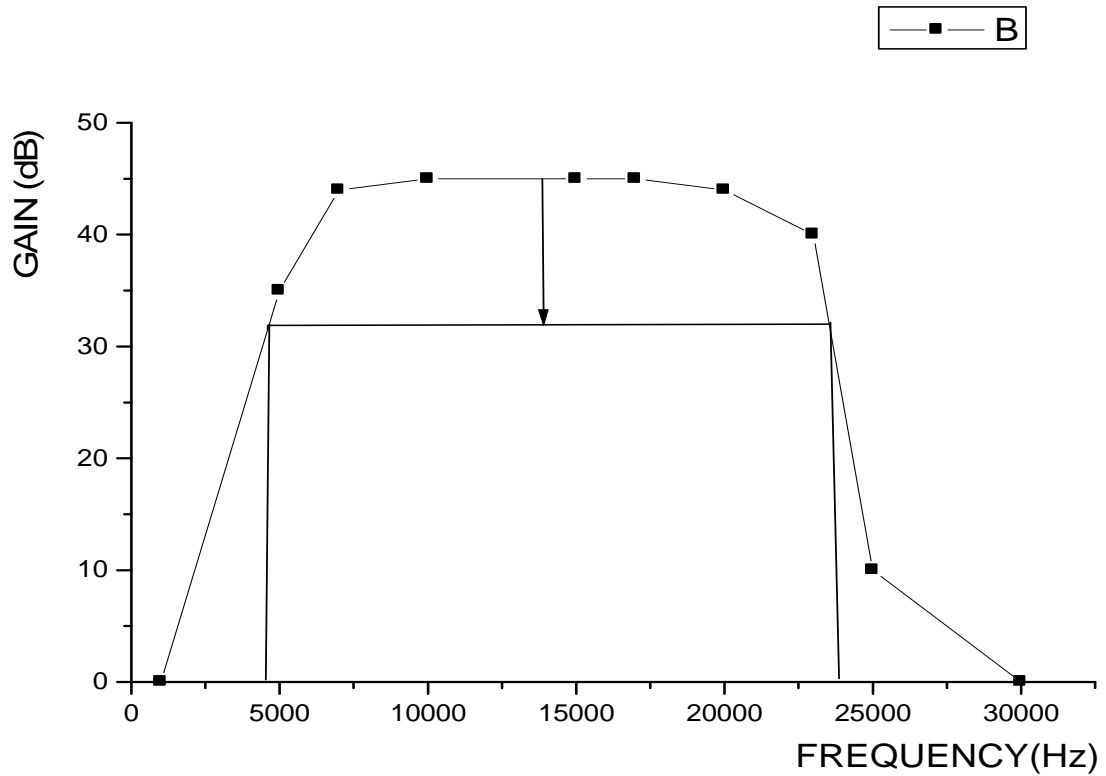


FIGURE 4.7 A graph of Gain (dB) against Frequency (Hz) for Common Emitter

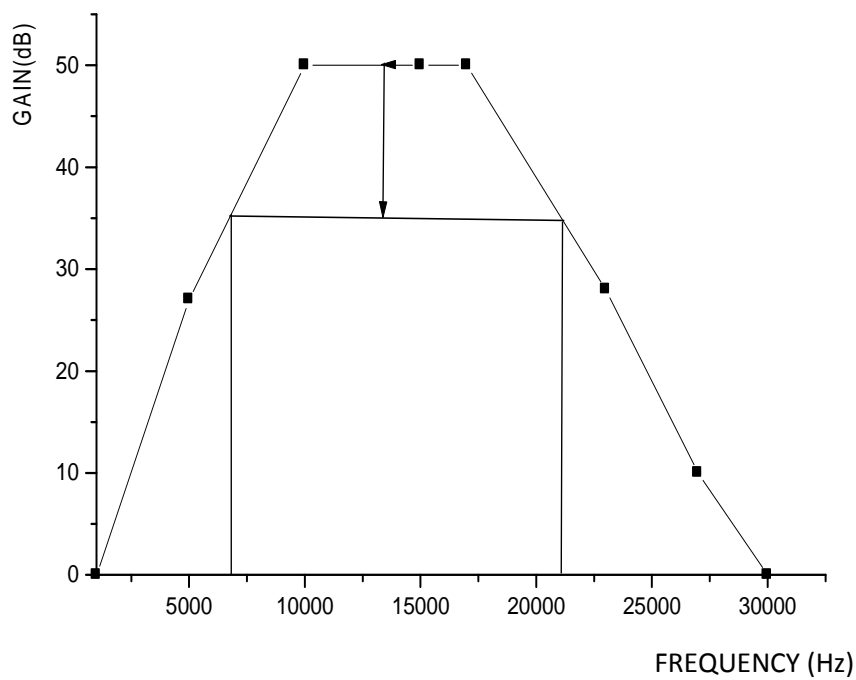


FIGURE 4.8 A graph of Gain (dB) against Frequency (Hz) for Emitter coupled before modification amplifier.

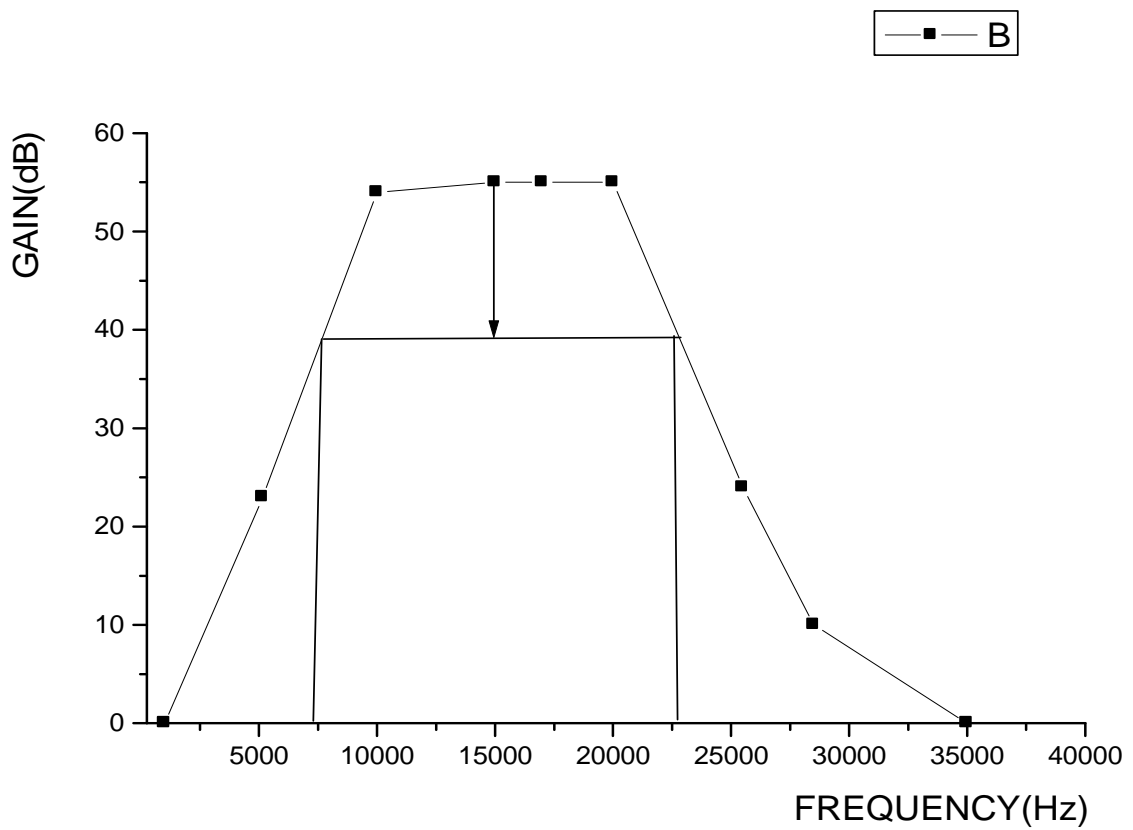


FIGURE 4.9 A graph of Gain (dB) against Frequency (Hz) for Emitter coupled after modification amplifier.

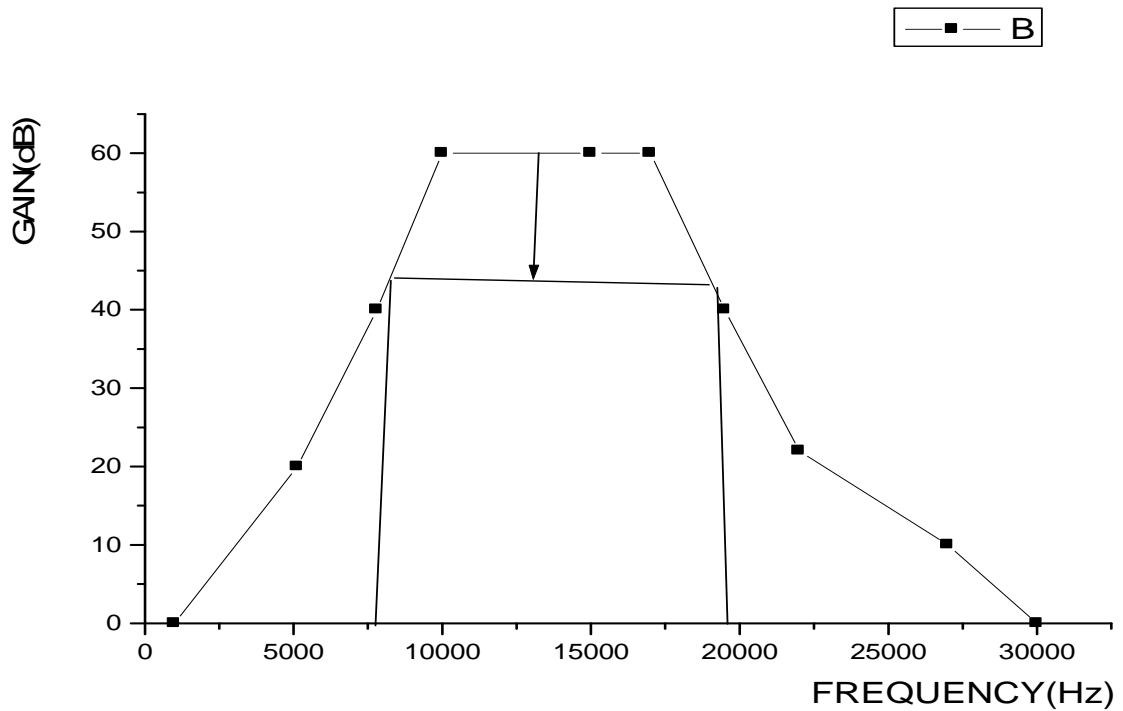


FIGURE 4.10 A graph of Gain (dB) against Frequency (Hz) for Cascaded Emitter coupled after modification amplifier.

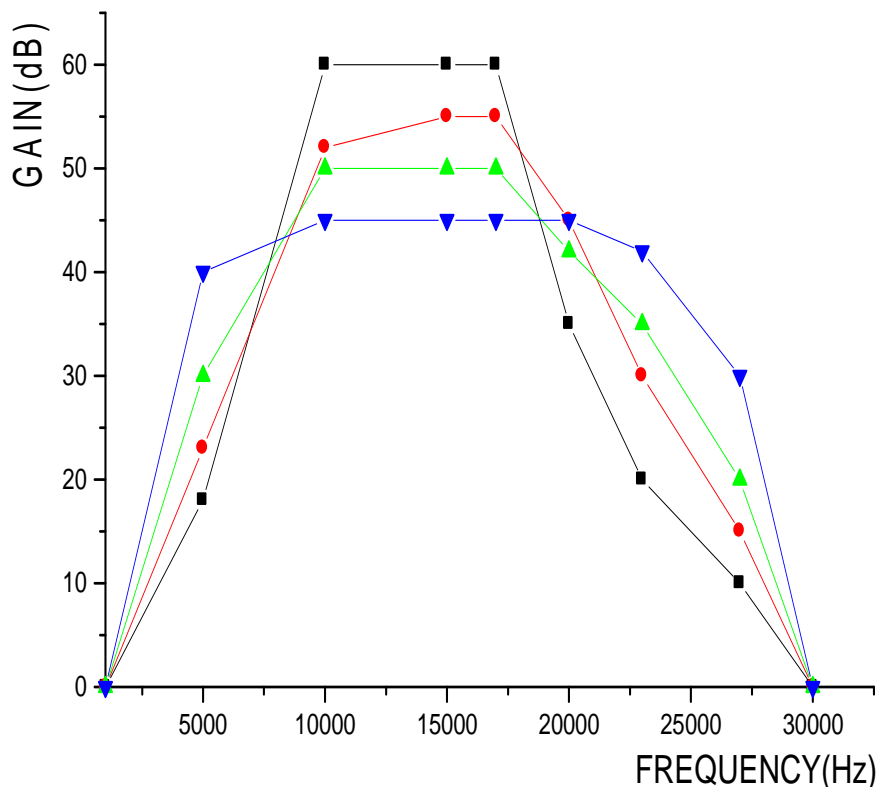


FIGURE 4.11 A Comparison graphs of Gain (dB) against Frequency (Hz) for Common Emitter, Emitter Coupled before modification, Emitter coupled after modification and Cascaded Emitter coupled after modification.

CONCLUSION

Within the range of simulation error the value of voltage gain of common emitter amplification, Emitter Coupled and cascaded Emitter Coupled were found to be greater than Unity, the common mode rejection ratio of this work was found to be half for all the values of amplification gain obtained. Also, from the comparative values, of simulation voltage gain of the designed amplifier was found to be 40 and that calculated from the circuit was found to be 46. Hence, the values were found to be closely related to one another.

REFERENCES

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- [2] Boylestad R.L. and Nashelsky L. Electronic Devices and Circuit Theory. (2006). 9th Edition Prentice-Hall, (India) New Delhi. P. 190-198.

The results shown that cascaded bandwidth was shrunk, while the overall gain was enhanced.

SUGGESTIONS

1. Selection of a wide range band of a transistor is highly recommendable.
2. A Quiescent Point (Q-Point) must be situated within a wide range of operation, for a good design amplifier.
3. Careful selection of the type of electronic workbench must be done, so as to overcome the simulation problem.

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[4] http://en.wikipedia.org/wiki/Differential_amplifier#Theory (22/12/2010)

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